Reference Current Distribution in MRAM Devices

ABSTRACT OF THE DISCLOSURE

A reference current distribution method and structure thereof for MRAM devices. An MRAM array includes current reference paths with substantially uniform length and resistance for all current paths flowing from the global reference current generator (GRCG) to a plurality of local current generators (LCGs), each LCG being coupled to at least one sub-array. The conductive wire segments that couple the LCGs to the GRCG are positioned such that all reference current path lengths from the GRCG to each LCG are substantially the same, ensuring that the resistance of all reference current paths is substantially the same and the amount of reference current provided by the GRCG to the LCGs is substantially the same. An advantage of an embodiment of present invention may be that the write margin is increased for the MRAM chip.